TSU2021 X21 Tester
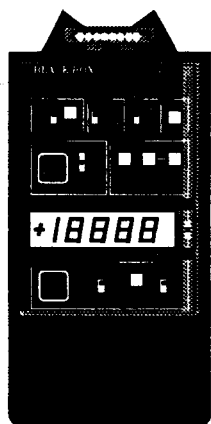
- Speed –up to 2.048Mb
- Clock Frequency measurement
- BERT (PRP15) generator / checker
- Master and Slave Timing options
- Clock Phasing error detection
- Data inversion detection
- LCD display – frequency / error counts
- Battery powered -typically 16 hours
- External 5V DC power input facility

X21 Interface Specifications

Pins (A + B)	In/Out	Signal
2 + 9	⇒	Transmit data
4 + 11	⇐	Received data
6 + 13	⇐	Clock in from DCE
3 + 10	⇒	Control
5 + 12	⇐	Indication
7 + 14	⇒	Clock out to DTE
8	⇔	Signal ground

Testing an X21 Circuit

Switch settings

Connect the TSU2021to the test interface via the cable supplied, which is terminated with a DB15 plug.

Set the **Transmit** to **PRP15** and set the clock source to **DCE** (clock must come from the attached interface).

Set the display switch to **Clock speed**, select **kbps**.

Input matching should be set to **110Ω** and **Ctrl** to **ON**.

BER testing

Switch on. If **Lo bat** flashes, replace the batteries.

Initially the unit will display the operational clock speed, which should be between 64 and 2048kbps. If the display remains blank apart from a hyphen, no clock has been detected and the BER test will not function.

The unit will automatically attempt to synchronise to another unit (or to itself, if the circuit has a data loop). While the PRP15 test is running, the left of the display will flash hyphen/colon alternately at a rate of 2Hz.

When the unit locks to a PRP15 test pattern (inverted, to meet ITU E1 PCM test requirements), it will display a green **PRP15 sync** LED. If the pattern is not inverted but otherwise correct, then a red sync indication will show: this implies a reversal in the receiver interface.

If there is any doubt about the polarity of the data, try transmitting either a constant binary 1 or 0 to the other end and likewise get the remote end to do the same.

Binary 1s cause the **Received data** LED to show red while 0s give a green indication. An alternating pattern of 1s and 0s causes this LED to show steady orange, while random data gives flickering orange-yellow.

Set the display switch to **Error count** to monitor and count any errors received. Move it to **rst** and back again to reset the count.

If a large number of errors is detected, check the **(PRP15 sync) lost** LED which indicates if there has been a loss of synchronisation owing to a circuit break or bad connection and causing an error burst.

Errors can be injected into the data stream, to verify that the tester is actually the source of the data, by pressing the **Inject error** button. If this is held down, errors will be generated at the rate of 2 per second.

Clock phasing

If the negative-going incoming clock edges are offset more than ±12.5% with respect to the centres of the data bits, the **Signal timing** LED will show red.

This shows that there may be a problem with the clock line, probably a reversal of the clock A/B wires in the interface cable. It may also indicate a bad connection in the cable or crosstalk on the cable itself.

Try switching the unit to **Hi-Z**. If the test functions correctly in this mode but not in the **110Ω** matched mode, you may either have one leg of the signal pair disconnected or problematic drivers on the attached equipment.

Connecting to a DTE interface

To test cabling up to and including a terminal device, provided that this can loop its data lines, the TSU2021can be configured to generate a clock. However, since the tester is itself a DTE, a DB15 female-to-female crossover adapter is needed, wired as follows:
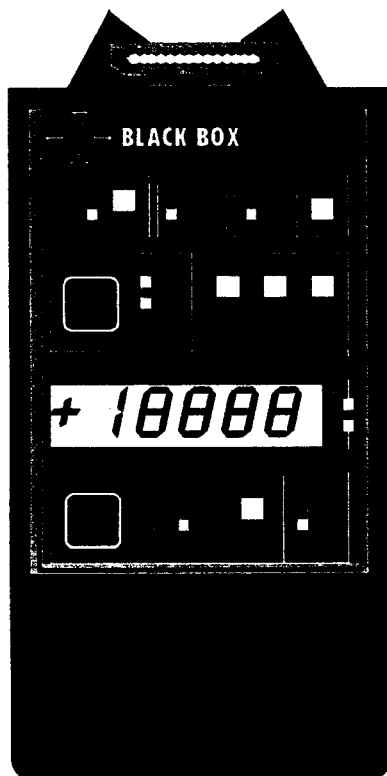
TSU2021i/f pin	External i/f pin
2	4
9	11
4	2
11	9
7	6
14	13
8	8
3	5
10	12
5	3
12	10

The TSU2021clock source must be set to **Tester**. Note that the DCE clock LED will stay out.

Set the display mode switch to **Clock speed** and press the **Set speed** button until the desired speed is indicated. The available clock rates are 64, 128, 256, 512, 1024 and 2048 kbps.

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Switches
  Power Off/On
  Input: Hi-Z or 110Ω
  Control : Sets condition of pins 3-10 to either an On or Off condition
  Transmit:
  Continuous 1's or 0's
  PRP15 test pattern-inverted as per ITU recommendation for 2.048Mb PCM systems
  PRP15 (2^{15}-1)
  Inject Errors: Single errors, hold for 2 errors / sec
  Error Count / Reset / Clock Speed
  Sets the display options for the LCD display
  Reset also resets the lost synch indicator
  Set Speed: Selects the appropriate clock speed to be output by the tester.
  Options (kbps): **64, 128, 256, 512, 1024 and 2048**
  DCE/Tester: sets the clock source to be used
  tester clock output on pins 7,14
  Kbps / n×64k: allows measured frequency to be divided by 64K to get channel multiple
LEDs
  Lo Battery(flashing): ≤ 30 mins power remaining
  Ind: displays the status of the indicate signal
  (pins 5 + 12), Red = Off, Green = ON
  Data: Red='1', Green='0'
  PRP sync: Green = OK, Red = inverted data
  Lost: indicates a loss of synchronisation has occurred during a test cycle-which may result in large error bursts.
  DCE: indicates status of clock signals
  Green – Clock phasing correct
  Red   – Clock phasing out of tolerance / inverted
LCD Display
  Inactive display shows a '-' sign
  PRP15 test operational: alternating '-' and ':' signs
  Overflow indicated by flashing most sig. '1'
  Error Display range 0000 to 19999
  Frequency display range: 1kHz – 2048kHz
  (rounded to the nearest whole kHz)
External Power Input
  1.3mm jack socket provided on Tester
  Power 5VDC – presented on female jack, tip +ve

Physical
Size   65×120×22mm (excluding connectors)
Weight   140g (5oz) approx (including batteries)
Case   ABS to UL-94H
Connector Keyed / locking IDC
Cable   Ribbon-approx 150mm

Power
Source   2 × AA cells (MnAlk recommended)
Life   typically 16 hours
External Stabilised 5VDC
          Both UK and Euro versions available
          301-0103 for UK version (3 pin)
          301-0104 for Euro plug version (2 pin)

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