Dual-Channel HS Sync/Async RS-232 Serial Interface

FEDERAL COMMUNICATIONS COMMISSION AND INDUSTRY CANADA
RADIO-FREQUENCY INTERFERENCE STATEMENTS

This equipment generates, uses, and can radiate radio-frequency energy and if not installed and used properly, that is, in strict accordance with the manufacturer's instructions, may cause interference to radio communication. It has been tested and found to comply with the limits for a Class A computing device in accordance with the specifications in Subpart J of Part 15 of FCC rules, which are designed to provide reasonable protection against such interference when the equipment is operated in a commercial environment. Operation of this equipment in a residential area is likely to cause interference, in which case the user at his own expense will be required to take whatever measures may be necessary to correct the interference.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

This digital apparatus does not exceed the Class A limits for radio noise emission from digital apparatus set out in the Radio Interference Regulation of Industry Canada.

Le présent appareil numérique n'émet pas de bruits radioélectriques dépassant les limites applicables aux appareils numériques de la classe A prescrites dans le Règlement sur le brouillage radioélectrique publié par Industrie Canada.

TRADEMARKS USED IN THIS MANUAL

Intel is a registered trademark of Intel Corporation.

Windows is a registered trademark or trademark of Microsoft Corporation in the United States and other countries.

PC/AT and OS/2 are registered trademarks, and PC/XT is a trademark, of International Business Machines Corporation.

Any other trademarks used in this manual are acknowledged to be the property of the trademark owners.

NORMAS OFICIALES MEXICANAS (NOM)
ELECTRICAL SAFETY STATEMENT

INSTRUCCIONES DE SEGURIDAD

1. Todas las instrucciones de seguridad y operación deberán ser leídas antes de que el aparato eléctrico sea operado.

2. Las instrucciones de seguridad y operación deberán ser guardadas para referencia futura.

3. Todas las advertencias en el aparato eléctrico y en sus instrucciones de operación deben ser respetadas.

4. Todas las instrucciones de operación y uso deben ser seguidas.

5. El aparato eléctrico no deberá ser usado cerca del agua—por ejemplo, cerca de la tina de baño, lavabo, sótano mojado o cerca de una alberca, etc..

6. El aparato eléctrico debe ser usado únicamente con carritos o pedestales que sean recomendados por el fabricante.

7. El parato eléctrico debe ser montado a la pared o al techo sólo como sea recomendado por el fabricante.

8. Servicio—El usuario no debe intentar dar servicio al equipo eléctrico más allá a lo descrito en las instrucciones de operación. Todo otro servicio deberá ser referido a personal de servicio calificado.

9. El aparato eléctrico debe ser situado de tal manera que su posición no interfiera su uso. La colocación del aparato eléctrico sobre una cama, sofá, alfombra o superficie similar puede bloquea la ventilación, no se debe colocar en libreros o gabinetes que impidan el flujo de aire por los orificios de ventilación.

10. El equipo eléctrico deber ser situado fuera del alcance de fuentes de calor como radiadores, registros de calor, estufas u otros aparatos (incluyendo amplificadores) que producen calor.

11. El aparato eléctrico deberá ser connectado a una fuente de poder sólo del tipo descrito en el instructivo de operación, o como se indique en el aparato.

12. Precaución debe ser tomada de tal manera que la tierra fisica y la polarización del equipo no sea eliminada.

13. Los cables de la fuente de poder deben ser guiados de tal manera que no sean pisados ni pellizcados por objetos colocados sobre o contra ellos, poniendo particular atención a los contactos y receptáculos donde salen del aparato.

14. El equio eléctrico debe ser limpiado únicamente de acuerdo a las recomendaciones del fabricante.

15. En caso de existir, una antena externa deberá ser localizada lejos de las lineas de energia.

16. El cable de corriente deberá ser desconectado del cuando el equipo no sea usado por un largo periodo de tiempo.

17. Cuidado debe ser tomado de tal manera que objectos liquidos no sean derramados sobre la cubierta u orificios de ventilación.

18. Servicio por personal calificado deberá ser provisto cuando:

   A: El cable de poder o el contacto ha sido dañado; u

   B: Objectos han caído o líquido ha sido derramado dentro del aparato; o

   C: El aparato ha sido expuesto a la lluvia; o

   D: El aparato parece no operar normalmente o muestra un cambio en su desempeño; o

   E: El aparato ha sido tirado o su cubierta ha sido dañada.

Contents

1. Specifications

Operating Requirements — IBM PC/XT™, PC/AT® or compatible running Windows®, DOS, or OS/2®

Number of Ports — Dual RS-232

Speed — Limited by RS-232 specification; typically 64 kbps

Connectors — (2) DB25 male

Maximum Distance — Up to 50 feet (15.2 m) @ 19.2 kbps per EIA RS-232 specifications

Communications Chip — 85230-8 SCC

MTBF — >150,000 hours

MTTR — <0.25 hours

Materials — Boards are solder mask over bare copper or tin nickel

Operating Temperature — 32 to 122°F (0 to 50°C)

Storage Temperature — -4 to +158°F (-20 to +70°C)

Humidity — 10 to 90% relative humidity, noncondensing

Power — +5 VDC @ 195 mA

Size — 4.9" x 4.2" (12.5 x 10.7 cm)

2. Introduction

2.1 Overview

The Dual-Channel HS Sync/Async RS-232 Serial Interface provides the PC with two direct synchronous/asynchronous links to RS-232 devices. The Dual-Channel HS Sync/Async RS-232 Serial Interface uses RS-232 connections with full modem clocking options. This provides an industry-standard interface to synchronous data links, modems, and other devices.

The software diskettes (included) contain utilities, diagnostics, and an example source code.

The disks' README file contains information about the latest changes and revisions. To view this file, insert the appropriate diskette into drive A or B and use Windows Notepad to read the READ.ME file. (In DOS, type `A:TYPE READ.ME|MORE [ENTER]` or `B:TYPE READ.ME|MORE [ENTER]`.)

2.2 What's Included

Your Serial Interface should come with the following items. If any of these items are missing or damaged, contact your supplier.

(1) Dual-Channel HS Sync/Async RS-232 Serial Interface,

(3) ACB software disks,

(1) Ribbon cable attached to a slot cover with a DB25 male connector

You will also need a shielded RS-232 cable (not included). We suggest using our part number EDN25C. Call for more information.

2.3 Features

• RS-232 interface modem control signals supported: TD, RD, RTS, CTS, DSR, DCD, DTR, TXC, RXC, and TT.

• DMA supports data rates greater than 1 million bps.

• Full-duplex DMA transfer capability.

- Software-programmable baud rate.

- Selectable port address, IRQ level (2-5) and DMA channels (1 or 3).

- Software developer's toolkit included with source code.

- High-speed Enhanced SCC (Z85230) compatible.

- Various oscillators available for custom clock rates. Call for more information.

2.4 Technical Description

The Dual-Channel HS Sync/Async RS-232 Serial Interface provides the PC with two high-speed sync/async ports. It can be used in a variety of sophisticated communications applications, such as SDLC, HDLC, X.25, bi-sync and high-speed async.

The Dual-Channel HS Sync/Async RS-232 Serial Interface uses the Zilog 85230 Serial Communications Controller (SCC). This chip features programmable baud rate, data format, interrupt control, and DMA control. Refer to the *Zilog Datacom I/O Handbook* or the *85230 Technical Manual* for details on programming the chip.

2.5 Programming the Dual-Channel HS Sync/Async RS-232 Serial Interface

Control/Status Port
The Dual-Channel HS Sync/Async RS-232 Serial Interface occupies eight Input/Output (I/O) addresses. The first four are used by the SCC chip, while the fifth address (Base+4) is the address of the on-board Control/Status Port. This port is used to set the Data Terminal Ready signal on or off, to enable or disable DMA under program control, and to monitor the Data Set Ready (DSR) signal from the modem. The following table lists bit positions of the Control/Status port. Note that status/control register bits 2 through 6 are not used.

Bit	Output Port Bits		Input Port Bits	
0	DTR A	1=ON, 0=OFF	DSR A	1=ON, 0=OFF
1	DTR B	1=ON, 0=OFF	DSR B	1=ON, 0=OFF
7	DMA Enable	1=ON, 0=OFF	Not Used	

Table 1. Status Register Examples.

Function	Program Bits
Turn On Ch. A DTR	Write Out Base+4, XXXX XXX1
Turn On Ch. B DTR	Write Out Base+4, XXXX XX1X
Turn Off Ch. A DTR	Write Out Base+4, XXXX XXX0
Turn Off Ch. B DTR	Write Out Base+4, XXXX XX0X
Enable DMA Drivers	Write Out Base+4, 1XXX XXXX
Disable DMA Drivers	Write Out Base+4, 0XXX XXXX
Test Ch. A DSR	Read In Base+4, Mask=0000 0001
Test Ch. B DSR	Read In Base+4, Mask=0000 0010

NOTE

Assembly-language programs should not do two successive I/O accesses, as this violates the 85230 SCC recovery-time specification. Refer to the 85230 technical reference for more details.

```
Correct:            Incorrect:
MOV DX,3E0H         MOV DX,3E0H
OUT DX,AL           OUT DX,AL
JMP $+2             OUT DX,AL
OUT DX,AL
```

Baud-Rate Generation
The baud rate of the SCC is programmed under software control. The standard oscillator supplied with the board is 7.3728 MHz. Other values may be substituted to achieve baud rates from 100 bps to 5 Mbps, as required, by replacing the oscillator (Y1).

Advanced Communication Board Software
ACB Developer Toolkit software provides sample software, DOS and Windows drivers, and technical insight to aid in the development of reliable applications and device drivers for the ACB family of communication cards. The goal in publishing this collection of source code and technical information is twofold: first, to provide the developer with ample information to develop ACB-based applications, and second, to provide a channel for your suggestions into our technical support efforts. The ACB Resource Kit provides a brief overview of the ACB product line. Topics concerning applications and integrations are covered to provide a complete overview of the ACB family. During your ACB development, if you have any questions, comments, or suggestions, contact Technical Support.

Direct Memory Access
Direct Memory Access (DMA) can be used to transfer data at very high rates. DMA allows the Interface to transfer data directly to or from system memory bypassing the CPU. The software examples provided on diskette demonstrate the setup and use of DMA.

P1 and P2 Connector

Table 2. P1 and P2 Connector Pinout.

Signal	Name	Pin #	Mode
GND	Ground	7	
RD	Receive Data	3	Input
CTS	Clear To Send	5	Input
DSR	Data Set Ready	6	Input
DCD	Data Carrier Detect	8	Output
TD	Transmit Data	2	Output
RTS	Request To Send	4	Output
TXC	Transmit Clock	15	Input/Output
RXC	Receive Clock	17	Input
TSET	Tx Signal Element Tim	24	Output
DTR	Data Terminal Ready	20	Output

NOTE

P1 is the DB25M on the card edge bracket for SCC Channel A.

P2 is the ribbon connector used for SCC Channel B.
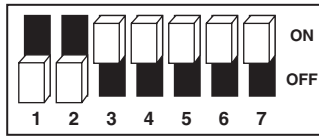
3. Address Selection

NOTE

Be sure to set the address selections and jumper options *before* installation.

The Dual-Channel HS Sync/Async RS-232 Serial Interface occupies 8 consecutive I/O locations. A DIP switch (SW2) is used to set the base addresses for these locations. It can reside in any I/O location between 100 and 3F8 hex. Be careful when selecting the base address, since some selections conflict with existing PC ports. The following table shows several examples that usually do not cause a conflict.

Address	Binary		Switch Position Setting (SW2)						
Hex	A9	A0	1	2	3	4	5	6	7
238-23F	1000111XXX		OFF	ON	ON	ON	OFF	OFF	OFF
280-287	1010000XXX		OFF	ON	OFF	ON	ON	ON	ON
2A0-2A7	1010100XXX		OFF	ON	OFF	ON	OFF	ON	ON
2E8-2EF	1011101XXX		OFF	ON	OFF	OFF	OFF	ON	OFF
300-307	1100000XXX		OFF	OFF	ON	ON	ON	ON	ON
328-32F	1100101XXX		OFF	OFF	ON	ON	OFF	ON	OFF
3E8-3EF	1111101XXX		OFF	OFF	OFF	OFF	OFF	ON	OFF

Typically COM1=3F8h; COM2=2F8h; COM3=3E8h; COM4=2E8h

The illustration on the next page shows the correlation between the DIP-switch setting and the address bits used to determine the base address. In the illustration, the address 300 hex through 307 hex is selected (300 hex = 1100000XXX in binary representation). Note that setting the switch ON (or closed) corresponds to a "0" in the address, while leaving it OFF (or open) corresponds to a "1."

The relative I/O addresses of the Dual-Channel HS Sync/Async RS-232 Serial Interface registers are as follows:

- Base+0   Channel A Data Port

- Base+1   Channel A Control Port

- Base+2   Channel B Data Port

- Base+3   Channel B Control Port

- Base+4   Board Control/Status Port

where "Base" is the selected board base address.

4. Option Selection

NOTE

Be sure to set the address selections and jumper options *before* installation.

The board contains several jumper straps which must be set for proper operation.

4.1 E8

E8 selects the interrupt request line (IRQ) for the Dual-Channel HS Sync/Async RS-232 Serial Interface. The diagram below shows IRQ 5 selected in shared configuration. If no interrupt is desired, remove the jumper.

2 3 4 5 N M

Jumper E8.

2	Selects IRQ2
3	Selects IRQ3
4	Selects IRQ4
5	Selects IRQ5
N	Selects Normal (1 IRQ per Board) IRQ Mode
M	Selects "Multi-IRQ" (Shared) IRQ Mode

The Factory-Default Setting for E8 is "5" and "M."

EPROM Usage

The EPROM socket is provided for convenience only and does not affect the communication functions of the board in any way. If the EPROM is not used, the socket should be disabled (DIP switch position 5 off). (See Figure 4-1.) The following table shows several EPROM base address examples.

The EPROM is a 27128 device occupying 16 KB of memory at or above C800 Hex that is recognized by the PC on bootup. Address lines A19, and A18 are always a binary 1, forcing a selection of C000 hex or greater.

Address	Address Lines				Switch Position Setting (SW1)			
	A17	A16	A15	A14	1	2	3	4
C000-C3FF	0	0	0	0	ON	ON	ON	ON
C400-C7FF	0	0	0	1	ON	ON	ON	OFF
C800-C9FF	0	0	1	0	ON	ON	OFF	ON
D000-D3FF	0	1	0	0	ON	OFF	ON	ON
D400-D7FF	0	1	0	1	ON	OFF	ON	OFF
D800-DBFF	0	1	1	0	ON	OFF	OFF	ON
E000-E3FF	1	0	0	0	OFF	ON	ON	ON
E400-E7FF	1	0	0	1	OFF	ON	ON	OFF

NOTE

Some AT class machines cannot use address E000 and above.

Figure 4-1 illustrates the correlation between the DIP-switch setting and the address bits used to determine the base address.

Switch position 5 enables and disables the EPROM socket. The default setting is with the EPROM socket disabled.

The Serial Interface is shipped with all the positions of SW1 turned off. If you use the EPROM socket, make sure you change the setting of SW1 to the address range you need.
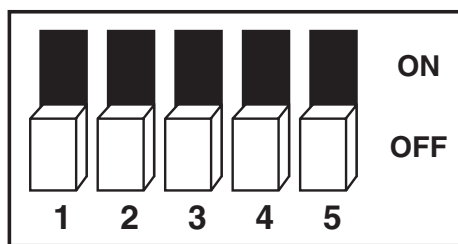
Figure 4-1. DIP Switch (SW1).

4.2 E11

E11 selects whether the EPROM (U21) is a 27128 (16K X 8) device, or a 27011 (16k x 8 x 8 pages) EPROM. Setting the jumper from 3 to 2 selects the 27128, while setting the jumper from 1 to 2 selects the 27011 EPROM.

NOTE

The 27011 EPROM is no longer available for distribution. This will however remain the factory-default configuration.
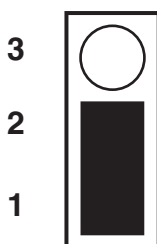

Figure 4-2. EPROM Device Type Selection (Factory Default is 1-2).

4.3 E4 and E5

These headers select the DMA mode of operation. Channel A of the SCC can be run in half-duplex or full-duplex DMA. Full duplex means that DMA can be used for simultaneous transmit and receive. Half-duplex DMA means that you can either transmit, or receive with DMA, but not in both directions simultaneously. You can use both channels A and B, in half-duplex mode, to transmit or receive, but not at the same time. The various options for E4 and E5 jumper settings are as follows:

NOTE

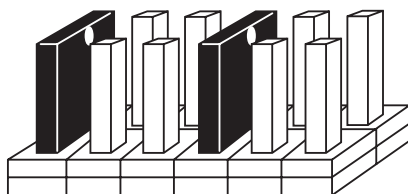**If DMA is not used, remove all of the jumpers on E4 and E5. Refer to Page 13 for the most common DMA settings.**

Figure 4-3. Header E4 DMA Options (Shown in Factory Default).

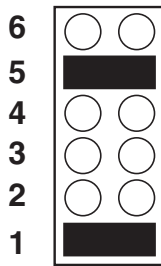| 6	DACK 1 DMA Acknowledge Channel 1
5	DACK 3 DMA Acknowledge Channel 3
4	ON = Ch. A Only/OFF = Ch. B Only
3	Two Channel A/B Mode A1B3
2	Two Channel A/B Mode A3B1
1	DACK 1 or 3 Acknowledge for Two-Channel Mode

Figure 4-4. Header E5 DMA Options (Shown in Factory Default).

6	SCC Channel A, DMA Channel 1 & 3 for Full Duplex Transfers
5	SCC Channel B Enable for Half Duplex DMA Transfers
4	SCC Channel A only can use DMA Ch.1
3	SCC Channel A or B can use DMA Ch. 1
2	SCC Channel A only can use DMA Ch. 3
1	SCC Channel A or B can use DMA Ch. 3

4.4 E9

Positions 1 and 2 enable or disable DMA operation. A jumper ON pos. 1 permanently enables the DMA tri-state drivers. A jumper ON pos. 2 places DMA under software control via the DMA enable control port (located at Base+4). *Removing the jumper disables the drivers and no DMA can be performed.*

NOTE

The power-on reset signal disables the DMA enable signal. A jumper placed in position 1 of E9 will override any software use of the DMA enable/disable status-port bit.

1	DMA Tri-state drivers permanently enabled
2	DMA Tri-State drivers enabled by status/control port bit 7

Figure 4-5. Header E9 DMA Enable (Shown in Factory Default).

Table 3. Commonly Used DMA Jumper Options.

Option	Jumpers on E4	Jumpers on E5	Program 85230
No DMA, Ch. A or B	None	None	N/A

Single-Channel DMA (Half-Duplex Only):

Option	Jumpers on E4	Jumpers on E5	Program 85230
Ch.A. DMA Ch. 1 Half-Duplex Ch. B No DMA	4, 6	4, 5	WAIT/REQ A
Ch.A. DMA Ch. 3 Half-Duplex Ch. B No DMA	4, 5	2, 5	WAIT/REQ A
Ch.B. DMA Ch. 1 Half-Duplex Ch. A No DMA	6 only	3, 5	WAIT/REQ B
Ch.B. DMA Ch. 3 Half-Duplex Ch. A No DMA	5 only	1, 5	WAIT/REQ B

Both DMA Channels (1 and 3) Selected:

Option	Jumpers on E4	Jumpers on E5	Program 85230
Ch. A DMA Ch. 1 Half-Duplex Ch. B DMA Ch. 3 Half-Duplex	1, 3	1, 4, 5	WAIT/REQ A WAIT/REQ B
Ch. A DMA Ch. 3 Half-Duplex Ch. B DMA Ch. 1 Half-Duplex	1, 2	2, 3, 5	WAIT/REQ A WAIT/REQ B

Full-Duplex Channel A with Both DMA Channels 1 and 3:

Option	Jumpers on E4	Jumpers on E5	Program 85230
Ch. A DMA Ch. 1 Receive Data Ch. A DMA Ch. 3 Transmit Data	1, 4	1, 4, 6	WAIT/REQ A DTR/REQ A
Ch. A DMA Ch. 3 Receive Data Ch. A DMA Ch. 1 Transmit Data	1, 4	2, 3, 6	WAIT/REQ A DTR/REQ A

NOTE

Channel B of the Dual-Channel HS Sync/Async RS-232 Serial Interface does not support full-duplex DMA.

Remember that E9 positions 1 and 2 enable or disable DMA operation.

4.5 E2 and E10

These jumpers set the input/output clock modes for the receive clock (RXC) and transmit clock (TXC) pins on the DB25 connector (pins 15 and 17). E2 sets the clock mode for the SCC Channel B (Port 2), while E10 sets the clock mode for the SCC Channel A (Port 1).

NOTE

The jumper for pin 17 must always be chosen as an input. It cannot be selected as an output as the SCC will not allow the RTXC pin to be programmed as an output.
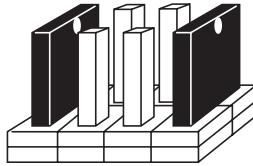

Figure 4-6. Header E2 and E10 (Shown in Factory Default).

O	Transmit Clock Output (15)
I	Transmit Clock Input (15)
O	N/A
I	Receive Clock Input (17)

4.6 E3 and E6

These jumpers also set the input/output clock modes for the transmit clock and the receive clock, as well as the signal source for terminal timing. E3 sets the clock mode for the SCC Channel B (Port 2), while E6 sets the clock mode for the SCC Channel A (Port 1).

NOTE

The jumper for the Receive Clock input/output (pins 5 and 6) must always be chosen as an input (pin 6). It cannot be selected as an output, because the SCC will not allow the RTXC pin to be programmed as an output.
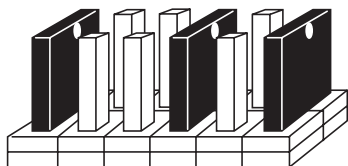
Figure 4-7. Header E3 and E6 (Shown in Factory Default).

1	Transmit Clock Output (TXC OUT)
2	Transmit Clock Input (TXC IN)
3	Terminal Timing—Sourced from SCC's TRXC pin or the input to TXC pin echoed to DB25 pin 24
4	Terminal Timing—The input to RXC pin is echoed to DB25 pin 24
5	Not Used
6	Receive Clock Input*

*These jumpers are always configured in this manner and should not be removed or replaced.

NOTE

The TXC pins (12 and 15) can be jumpered as either in input or an output. The TSET pins (11 and 24) will always echo the TXC pins, regardless of whether the TXC pins are selected as an input or an output.

5. Installation

NOTE

Be sure to set the address selections and jumper options *before* installation.

The Dual-Channel HS Sync/Async RS-232 Serial Interface can be installed in any of the PC expansion slots except J8 on the XT and portable.

1. Turn off the PC's power. Disconnect the power cord.

2. Remove the PC case cover.

3. Locate two available slots and remove the blank metal slot covers.

4. Install the Channel B cable in Box Header E1. This cable is keyed to prevent improper installation. Gently insert the Dual-Channel HS Sync/Async RS-232 Serial Interface into the slot. Make sure it's seated properly. Attach the cable to the adjacent slot with the retaining screw. (If Channel B of the Dual-Channel HS Sync/Async RS-232 Serial Interface is not used, the adapter cable is not required.)

5. Replace the cover.

6. Reconnect the power cord.

Installation is complete.

6. Troubleshooting

Use the supplied ACB software, along with these instructions, to help eliminate some common problems that you may encounter.

1) Identify all I/O adapters currently installed in your system. This includes your onboard serial ports, controller cards, and sound cards. The addresses used by these adapters, as well as the IRQ, should be identified.

2) Configure your Serial Interface so that there is no conflict with currently installed adapters. No two adapters can occupy the same I/O adapters.

3) Make sure the Interface is using a unique IRQ. While the Interface does allow the sharing of IRQs, many other adapters (such as SCSI adapters and onboard serial ports) do not. The IRQ is typically selected via an onboard header block. Refer to **Chapters 3** and **4** for help in choosing an I/O address and IRQ.

4) Make sure the Serial Interface is securely installed in a motherboard slot.

5) If you are using DOS, use the supplied DOS diskette and this manual to verify that the Interface Card is configured correctly. The diskette contains a diagnostic program, SSDACB, that will verify if the Interface is configured correctly. Refer to the UTIL.TXT file found in the \UTIL sub-directory on the disk for detailed instructions on using SSDACB.

If you're using Windows 95, 98, or Windows NT, use one of the other diskettes. Call Tech Support if you need help with proper configuration and installation.

6) The following are known I/O conflicts:
   • The 278 and 378 settings may conflict with your printer I/O adapter.
   • 3B0 cannot be used if a monochrome adapter is installed.
   • 3F8-3FF is typically reserved for COM1.
   • 2F8-2FF is typically reserved for COM2.
   • 3E8-3EF is typically reserved for COM3.
   • 2E8-2EF is typically reserved for COM4. This is a valid setup option for the Card. However, since only 10 address lines are actually decoded, a possible conflict with an advanced video card emulating the IBM XGA adapter (8514 register set) may occur.

Appendix A: Circuit-Board Design
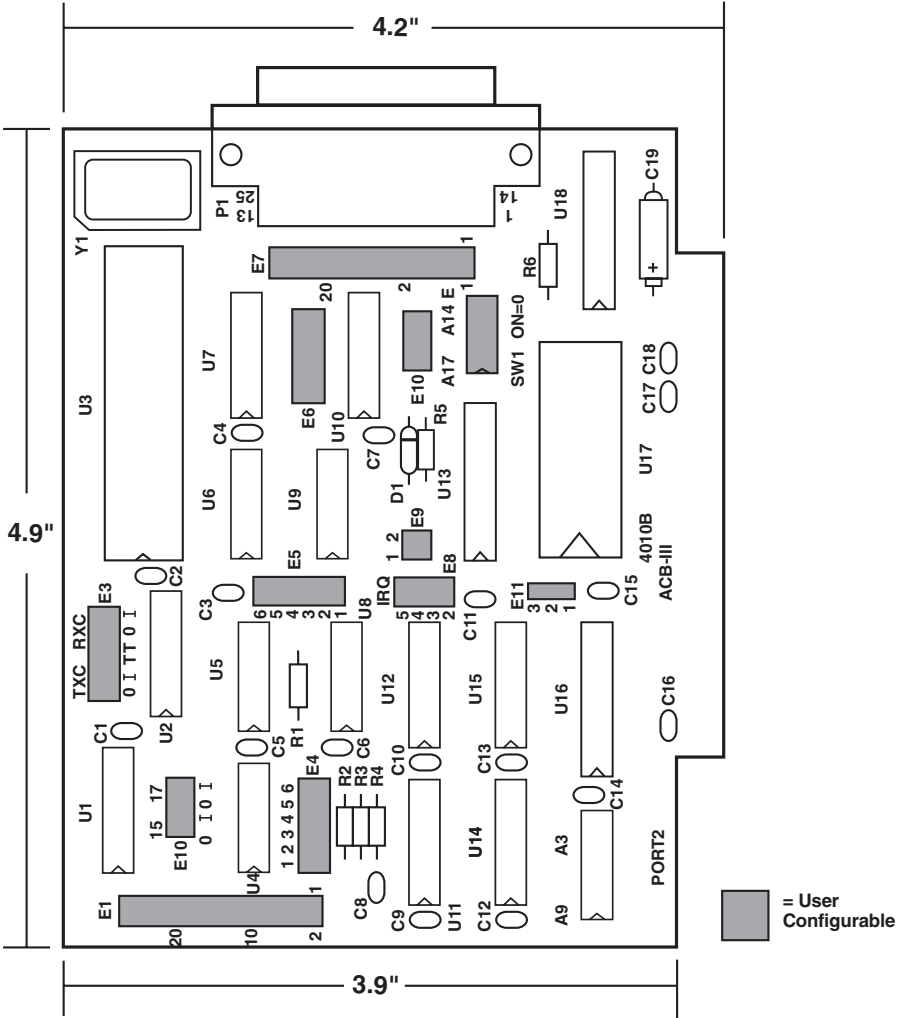
Appendix B: The RS-232 Interface

RS-232 is the most widely used communication standard. It has been defined and revised several times and is often referred to as EIA/TIA-232. It is defined by the EIA as the "Interface Between Data Terminal Equipment and Data Circuit-Terminating Equipment Employing Serial Binary Data Interchange."

The mechanical implementation of RS-232 is on a 25-pin D-sub connector. The IBM AT computer defined the RS-232 port on a 9-pin D-sub connector and subsequently the EIA/TIA approved this implementation as the EIA/TIA-574 standard. This standard is defined as the "9-Position Non-Synchronous Interface Between Data Terminal Equipment and Data Circuit-Terminating Equipment Employing Serial Binary Data Interchange." Both implementations are in widespread use and will be referred to as RS-232.

RS-232 is capable of operating at data rates up to 20 kbps at distances less than 50 feet. The absolute maximum data rate may vary because of line conditions and cable lengths. RS-232 often operates at 38.4 kbps over very short distances.

The voltage levels defined by RS-232 range from -12 to +12 volts. RS-232 is a single-ended or unbalanced interface, meaning that a single electrical signal is compared to a common signal (ground) to determine binary logic states. A voltage of +12 volts (usually +3 to +10 volts) represents a binary 0 (space), and -12 volts (-3 to -10 volts) denotes a binary 1 (mark).

The RS-232 and the EIA/TIA-574 specification defines two types of interface circuits, Data Terminal Equipment (DTE) and Data Circuit-Terminating Equipment (DCE). The Dual-Channel HS Sync/Async RS-232 Serial Interface is an RS-232 synchronous DTE interface.

Appendix C: Direct Memory Access

In many instances it is necessary to transmit and receive data at greater rates than would be possible with simple port I/O. In order to provide a means for faster data transfers, a special function called Direct Memory Access (DMA) was built into the original IBM PC. The DMA function allows the Dual-Channel HS Sync/Async RS-232 Serial Interface (or any other DMA compatible interface) to read or write data to or from memory without using the microprocessor. This function was originally controlled by the Intel 8237 DMA controller chip, but may now be a combined function of the peripheral support chip sets (for example, Chips & Technology or Symphony chip sets).

During a DMA cycle, the DMA controller chip, not the microprocessor, is driving the system bus. When an interface needs to use DMA, it activates a DMA request signal (DRQ) to the DMA controller, which in turn sends a DMA hold request to the microprocessor. When the microprocessor receives the hold request, it will respond with an acknowledge to the DMA controller chip. The DMA controller chip then becomes the owner of the system bus, providing the necessary control signals to complete a memory-to-I/O or I/O-to-memory transfer. When the data transfer is started, an acknowledge signal (DACK) is sent by the DMA controller chip to the Dual-Channel HS Sync/Async RS-232 Serial Interface. Once the data has been transferred to or from the Dual-Channel HS Sync/Async RS-232 Serial Interface, the DMA controller returns control to the microprocessor.

To use DMA with the Dual-Channel HS Sync/Async RS-232 Serial Interface requires a thorough understanding of the PC DMA functions. The ACB Developers Toolkit demonstrates the setup and use of DMA with several source-code and high-level language demo programs.

Appendix D: Async and Sync Communications

In serial data communications, individual bits of a character are transmitted consecutively to a receiver that assembles the bits back into a character. Data rate, error checking, handshaking, and character framing (start/stop bits or sync characters) are pre-defined and must correspond at both the transmitting and receiving ends. The techniques used for serial communications can be divided into two groups: asynchronous and synchronous.

The main difference between asynchronous and synchronous serial communications is how each method defines the beginning and end of a character or group of characters. The method of determining the duration of each bit in the data stream is also an important difference.

Asynchronous Communications

Asynchronous communications is the standard means of serial data communication for PC compatibles and PS/2 computers. The original PC was equipped with a communication or COM port that was designed around an 8250 Universal Asynchronous Receiver Transmitter (UART). This device allows asynchronous serial data to be transferred through a simple and straightforward programming interface. Character boundaries for asynchronous communications are defined by a starting bit followed by a pre-defined number of data bits (5, 6, 7, or 8). The end of the character is defined by the transmission of a pre-defined number of stop bits (usually 1, 1.5, or 2).
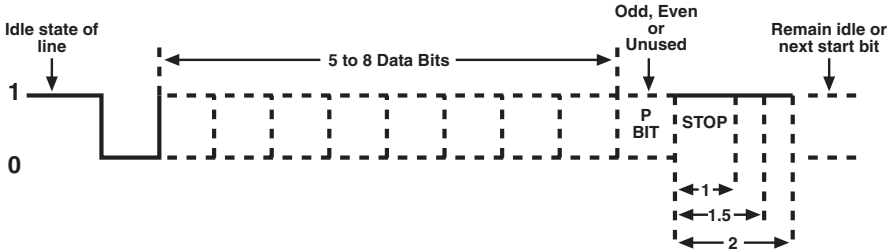
Figure D-1. Asynchronous Communications Bit Diagram.

An extra bit used for error detection is often appended before the stop bits. This special bit is called the parity bit. Parity is a simple method of determining if a data bit has been lost or corrupted during transmission. There are several methods for implementing a parity check to guard against data corruption. Common methods are called (E)ven Parity or (O)dd Parity. Sometimes parity is not used to detect errors on the data stream. This is referred to as (N)o parity.

Because each bit in asynchronous communications is sent consecutively, it is easy to generalize asynchronous communications by stating that each character is wrapped (framed) by pre-defined bits to mark the beginning and end of the serial transmission of the character. The communication parameters for asynchronous communications have to be the same at both the transmitting and receiving ends. The communication parameters are baud rate, parity, number of data bits per character, and stop bits (for example, 9600, N, 8, 1).

Synchronous Communications

Synchronous communications is used for applications that require higher data rates and better error-checking procedures. Bit duration in synchronous communications is not necessarily pre-defined at both the transmitting and receiving ends. Typically, in addition to the data signal, a clock signal is provided. This clock signal will mark the beginning of a bit cell on a pre-defined transmission. The source of the clock is predetermined and sometimes multiple clock signals are available. For example, if two nodes want to establish synchronous communications, point A could supply a clock to point B that would define all bit boundaries that A transmitted to B. Point B could also supply a clock to point A that would correspond to the data that A received from B. This example demonstrates how communications could take place between two nodes at completely different data rates.

Character synchronization with synchronous communications is also very different from the asynchronous method of using start and stop bits to define the beginning and end of a character. In synchronous communications, a pre-defined character or sequence of characters is used to let the receiving end know when to start character assembly.

This pre-defined character is called a sync character or sync flag. Once the sync flag is received, the communications device will start character assembly. Sync characters are typically transmitted while the communications line is idle or immediately before a block of information is transmitted. To illustrate with an example, assume that we are communicating using eight bits per character. Point A is receiving a clock from point B and sampling the receive data pin on every upward clock transition. Once point A receives the pre-defined bit pattern (sync flag), the next eight bits are assembled into a valid character. The following eight bits are also assembled into a character. This will repeat until another pre-defined sequence of bits is received (either another sync flag or a bit combination that signals the end of the text, e.g., EOT). The actual sync flag and protocol varies depending on the sync format (SDLC, BISYNC, etc.).

BLACK BOX®
NETWORK SERVICES

1000 Park Drive   •   Lawrence, PA 15055-1018   •   724-746-5500   •   Fax 724-746-0746

Addendum
Dual-Channel HS Sync/Async
RS-232 Serial Interface

This addendum contains important changes to your October 1997 Dual-Channel HS Sync/Async RS-232 Serial Interface manual. Please keep this addendum with that manual for easy reference.

On page 6 (and then throughout the manual), we refer to an ACB Developer Toolkit diskette. At the time of that manual printing, only one diskette was included. Now, however, 3 diskettes are included. One diskette is for DOS users, and the other two are for Windows 95, 98, or Windows NT users.

We're sorry for any inconvenience this may have caused. If you have any questions about how to use the diskettes, please contact Technical Support.

**CUSTOMER
SUPPORT
INFORMATION**

Order **toll-free** in the U.S. 24 hours, 7 A.M. Monday to midnight Friday: **877-877-BBOX**
FREE technical support, 24 hours a day, 7 days a week: Call **724-746-5500** or fax **724-746-0746**
Mail order: **Black Box Corporation**, 1000 Park Drive, Lawrence, PA 15055-1018
Web site: **www.blackbox.com** • E-mail: **info@blackbox.com**