Dual Channel HS Sync/Async V.35 Serial Interface

FEDERAL COMMUNICATIONS COMMISSION
AND
INDUSTRY CANADA
RADIO FREQUENCY INTERFERENCE STATEMENTS

This equipment generates, uses, and can radiate radio frequency energy and if not installed and used properly, that is, in strict accordance with the manufacturer's instructions, may cause interference to radio communication. It has been tested and found to comply with the limits for a Class A computing device in accordance with the specifications in Subpart J of Part 15 of FCC rules, which are designed to provide reasonable protection against such interference when the equipment is operated in a commercial environment. Operation of this equipment in a residential area is likely to cause interference, in which case the user at his own expense will be required to take whatever measures may be necessary to correct the interference.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

This digital apparatus does not exceed the Class A limits for radio noise emission from digital apparatus set out in the Radio Interference Regulation of Industry Canada.

Le présent appareil numérique n'émet pas de bruits radioélectriques dépassant les limites applicables aux appareils numériques de la classe A prescrites dans le Règlement sur le brouillage radioélectrique publié par Industrie Canada.

NORMAS OFICIALES MEXICANAS (NOM)
ELECTRICAL SAFETY STATEMENT

INSTRUCCIONES DE SEGURIDAD

1. Todas las instrucciones de seguridad y operación deberán ser leídas antes de que el aparato eléctrico sea operado.

2. Las instrucciones de seguridad y operación deberán ser guardadas para referencia futura.

3. Todas las advertencias en el aparato eléctrico y en sus instrucciones de operación deben ser respetadas.

4. Todas las instrucciones de operación y uso deben ser seguidas.

5. El aparato eléctrico no deberá ser usado cerca del agua—por ejemplo, cerca de la tina de baño, lavabo, sótano mojado o cerca de una alberca, etc..

6. El aparato eléctrico debe ser usado únicamente con carritos o pedestales que sean recomendados por el fabricante.

7. El aparato eléctrico debe ser montado a la pared o al techo sólo como sea recomendado por el fabricante.

8. Servicio—El usuario no debe intentar dar servicio al equipo eléctrico más allá a lo descrito en las instrucciones de operación. Todo otro servicio deberá ser referido a personal de servicio calificado.

9. El aparato eléctrico debe ser situado de tal manera que su posición no interfiera su uso. La colocación del aparato eléctrico sobre una cama, sofá, alfombra o superficie similar puede bloquea la ventilación, no se debe colocar en libreros o gabinetes que impidan el flujo de aire por los orificios de ventilación.

10. El equipo eléctrico deber ser situado fuera del alcance de fuentes de calor como radiadores, registros de calor, estufas u otros aparatos (incluyendo amplificadores) que producen calor.

11. El aparato eléctrico deberá ser connectado a una fuente de poder sólo del tipo descrito en el instructivo de operación, o como se indique en el aparato.

12. Precaución debe ser tomada de tal manera que la tierra fisica y la polarización del equipo no sea eliminada.

13. Los cables de la fuente de poder deben ser guiados de tal manera que no sean pisados ni pellizcados por objetos colocados sobre o contra ellos, poniendo particular atención a los contactos y receptáculos donde salen del aparato.

14. El equipo eléctrico debe ser limpiado únicamente de acuerdo a las recomendaciones del fabricante.

15. En caso de existir, una antena externa deberá ser localizada lejos de las lineas de energia.

16. El cable de corriente deberá ser desconectado del cuando el equipo no sea usado por un largo periodo de tiempo.

17. Cuidado debe ser tomado de tal manera que objectos liquidos no sean derramados sobre la cubierta u orificios de ventilación.

18. Servicio por personal calificado deberá ser provisto cuando:

   A: El cable de poder o el contacto ha sido dañado; u

   B: Objectos han caído o líquido ha sido derramado dentro del aparato; o

   C: El aparato ha sido expuesto a la lluvia; o

   D: El aparato parece no operar normalmente o muestra un cambio en su desempeño; o

   E: El aparato ha sido tirado o su cubierta ha sido dañada.

Contents

1. Specifications

Operating Requirements — IBM® PC/XT™, AT, or compatible running DOS, Windows™, or OS/2®

Number of Ports — Dual V.35

Communications Chip — 85230-8 SCC

Speed — 1.2288 Mbps

Connectors — DB15 male

Maximum Distance — Up to 5000 feet (1524 m) @ 9600 bps

MTBF — >150,000 hours

MTTR — <0.25 hours

Materials — Boards are solder mask over bare copper

Operating Temperature — 32 to 122°F (0 to 50°C)

Storage Temperature — -4 to +158°F (-20 to +70°C)

Humidity — Up to 90% relative humidity, noncondensing

Power — +5 V @ 450 mA, -5 V @ 75 mA, ±12V @ 50 mA ea.

Size — ¾-inch card

2. Introduction

2.1 Overview

The Dual Channel HS Sync/Async V.35 Serial Interface provides the PC with two high-speed synchronous/asynchronous links to devices requiring extremely fast data flow. The Dual Channel HS Sync/Async V.35 Serial Interface incorporates the V.35 connector specification relying on balanced twisted-pair cabling from the board to the external device.

The software diskette (included) contains utilities, diagnostics, and an example source code.

The README file on the disk contains information about the latest changes and revisions. To view this file, insert the diskette into drive A or B and type `A:TYPE READ.ME|MORE [ENTER]` or `B:TYPE READ.ME|MORE [ENTER]`.

2.2 What's Included

Your Serial Interface should come with the following items. If any of these items are missing or damaged, contact your supplier.

(1) Dual Channel HS Sync/Async V.35 Serial Interface,

(1) ACB Developer Toolkit Disk,

(1) DB15-to-V.35 cable,

This manual

2.3 Features

Listed below are the special features your Serial Interface offers.

• CCITT V.35 interface with full modem control, supports TD, RD, RTS, CTS, DSR, DCD, DTR, TXC, and RXC signals.

• DMA supports data rates greater than 1 million bps.

• Full-duplex DMA transfer capability.

• Software-programmable baud rate.

• Selectable port address, IRQ level (2-5) and DMA channels (1 or 3).

• Software developer's toolkit included with source code.

• High-speed Enhanced SCC (85C30, 85230) compatible.

• Various oscillators available for custom clock rates. Call your supplier for more information.

2.4 Technical Description

The Dual Channel HS Sync/Async V.35 Serial Interface provides the PC with two high-speed sync/async ports. It can be used in a variety of sophisticated communications applications, such as SDLC, HDLC, X.25, and high-speed async.

The Dual Channel HS Sync/Async V.35 Serial Interface utilizes the Zilog® 85230 Serial Communications Controller (SCC). This chip features programmable baud rate, data format, interrupt control, and DMA control. Refer to the Zilog SCC user's manual and the ACB Developer's Toolkit diskette for details on programming the SCC chip.

CCITT V.35
The Comite Consultatif Internationale de Telegraphie et Telephonie also known as the CCITT is the agency that established the V.35 standard. V.35 specifies an electrical, mechanical, and physical interface that is used extensively by high-speed digital carriers such as AT&T® Dataphone® Digital Service (DDS). CCITT V.35 is an international standard that is often referred to as "Data Transmission at 48 Kbps Using 60-108 KHz Group-Band Circuits."

CCITT V.35 electrical characteristics are a combination of unbalanced voltage and balanced current mode signals. Data and clock signals are balanced current mode circuits. These circuits typically have voltage levels from 0.5 Volts to -0.5 Volts (1 Volt differential). The modem control signals are unbalanced signals and are compatible with RS-232.

The physical connector is a 34-pin connector that supports 24 data, clock, and control signals. It is defined in the ISO-2593 standard.

CCITT V.35 is implemented with both DTE and DCE interfaces: the Dual Channel HS Sync/Async V.35 Serial Interface is implemented using the DTE interface.

The Dual Channel HS Sync/Async V.35 Serial Interface will not generate a clock signal without a modification. This is because the CCITT V.35 specification does not specify a clock output signal for a V.35 DTE. If you require an output clock signal with your V.35 interface, call your supplier.

The Dual Channel HS Sync/Async V.35 Serial Interface is also compatible with CCITT V.36 and V.37.

2.5 Programming the Dual Channel HS Sync/Async V.35 Serial Interface

Control/Status Port

The Dual Channel HS Sync/Async V.35 Serial Interface occupies eight Input/Output (I/O) addresses. The first four are used by the SCC chip, while the fifth address (Base+4) is the address of the on-board Control/Status Port. This port is used to set the Data Terminal Ready (DTR) signal, to enable or disable DMA under software control, and to monitor the Data Set Ready (DSR) input signals from the modem. The following table lists bit positions of the Control/Status port.

Bit	Output Port Bits		Input Port Bits	
0	DTR A	1=ON, 0=OFF	DSR A	1=OFF, 0=ON
1	DTR B	1=ON, 0=OFF	DSR B	1=OFF, 0=ON
2	Not Used		Not Used	1=OFF, 0=ON
3	Not Used		Not Used	1=OFF, 0=ON
4	Not Used		Not Used	1=OFF, 0=ON
5	Not Used		Not Used	1=OFF, 0=ON
6	Not Used		Not Used	1=OFF, 0=ON
7	DMA Enable	1=ON, 0=OFF	Not Used	1=OFF, 0=ON

Function	Program Bits
Turn On Ch. A DTR	Write Out Base+4, XXXX XXX1
Turn On Ch. B DTR	Write Out Base+4, XXXX XX1X
Turn Off Ch. A DTR	Write Out Base+4, XXXX XXX0
Turn Off Ch. B DTR	Write Out Base+4, XXXX XX0X
Enable DMA Drivers	Write Out Base+4, 1XXX XXXX
Disable DMA Drivers	Write Out Base+4, 0XXX XXXX
Test Ch. A DSR	Read In Base+4, Mask=0000 0001
Test Ch. B DSR	Read In Base+4, Mask=0000 0010

NOTE

Assembly-language programs should not do two successive I/O accesses, as this violates the 85230 SCC recovery-time specification. Refer to the 85230 technical reference for more details.

```
Correct:              Incorrect:
MOV DX,3E0H           MOV DX,3E0H
OUT DX,AL             OUT DX,AL
JMP $+2               OUT DX,AL
OUT DX,AL
```

Direct Memory Access
Direct Memory Access (DMA) can be used to transfer data at very high rates. DMA allows the Serial Interface to transfer data directly to or from system memory, bypassing the CPU. The software examples provided on diskette demonstrate the setup and use of DMA.

Advanced Communication Board Developer Toolkit Diskette and the ACB Resource Kit
The diskette provides sample software and technical insight to aid in the development of reliable applications and device drivers based on the ACB family of communication cards. The goal in publishing this collection of source code and technical information is twofold: first, to provide the developer with ample information to develop ACB-based applications, and second, to provide a channel for suggestions into our technical support efforts. The ACB Resource Kit provides a brief overview of the ACB product line. Topics concerning applications and integration are covered to provide a complete overview of the ACB family. During your ACB development, if you have any questions, comments, or suggestions, contact Technical Support.

Internal Baud-Rate Generator
The baud rate of the SCC is programmed under software control. The standard oscillator supplied with the board is 7.3728 MHz. Other values may be substituted to achieve different baud rates.

P1 and P2 Connector
The connector on the Serial Interface is a DB15. This connector is then matched with a V.35 cable to provide the proper mechanical connection as required by the ISO-2593 standard.

NOTE

The connector for the SCC Channel A is labeled as P2; it's the bottom connector when the card is installed in a socket. The connector for SCC Channel B is labeled P1; it's the top connector when the card is installed in a socket.

Table 1. P1 and P2 Connector Pinout

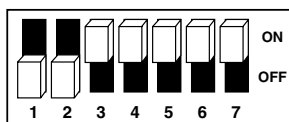| Signal		Name	DB15 Pin #	V.35 Pin #	Mode
GND		Ground	8	B	
TDB	TX+	Transmit Data Positive	2	S	Output V.35
TDA	TX-	Transmit Data Negative	9	P	Output V.35
RDB	RX+	Receive Data Positive	4	T	Input V.35
RDA	RX-	Receive Data Negative	11	R	Input V.35
TXCB	TXC+	Transmit Clock Positive	12	AA	Input V.35
TXCA	TXC-	Transmit Clock Negative	10	Y	Input V.35
RXCB	RXC+	Receive Clock Positive	13	X	Input V.35
RXCA	RXC-	Receive Clock Negative	14	V	Input V.35
CTS	CTS	Clear To Send	5	D	Input RS-232
DSR	DSR	Data Set Ready	6	E	Input RS-232
DCD	DCD	Data Carrier Detect	7	F	Input RS-232
RTS	RTS	Request To Send	3	C	Output RS-232
DTR	DTR	Data Terminal Ready	15	H	Output RS-232

3. Address Selection

NOTE

Be sure to set the address selections and jumper options *before* installation.

The Dual Channel HS Sync/Async V.35 Serial Interface occupies 8 consecutive I/O locations. A DIP switch (SW1) is used to set the base address for these locations. Be careful when selecting the base address, since some selections conflict with existing PC ports. The following table shows several examples that usually do not cause a conflict.

Address	Binary		Switch Position Setting						
Hex	A9	A0	1	2	3	4	5	6	7
238-23F	1000111XXX		OFF	ON	ON	ON	OFF	OFF	OFF
280-287	1010000XXX		OFF	ON	OFF	ON	ON	ON	ON
2A0-2A7	1010100XXX		OFF	ON	OFF	ON	OFF	ON	ON
2E8-2EF	1011101XXX		OFF	ON	OFF	OFF	OFF	ON	OFF
300-307	1100000XXX		OFF	OFF	ON	ON	ON	ON	ON
328-32F	1100101XXX		OFF	OFF	ON	ON	OFF	ON	OFF
3E8-3EF	1111101XXX		OFF	OFF	OFF	OFF	OFF	ON	OFF

Typically COM1:=3F8h; COM2:=2F8h; COM3:=3E8h; COM4:=2E8h

The following illustration shows the correlation between the DIP switch setting and the address bits used to determine the base address. In the figure below, the address 300 hex through 307 hex is selected (300 hex =11 0000 0XXX in binary representation). Note that setting the switch ON (or closed) corresponds to a "0" in the address, while leaving it OFF (or open) corresponds to a "1."

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The relative I/O addresses of the 85230 SCC registers are as follows:

- Base+0   Channel A Data Port

- Base+1   Channel A Control Port

- Base+2   Channel B Data Port

- Base+3   Channel B Control Port

- Base+4   Board Control/Status Port

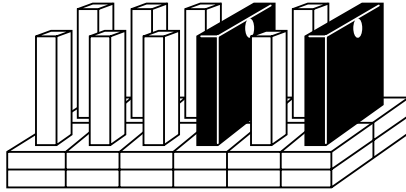where "Base" is the selected board base address.

4. Option Selection

NOTE

Be sure to set the address selections and jumper options *before* installation.

The board contains several jumper straps which must be set for proper operation.

4.1 E3

E3 selects the interrupt request line for the port. The diagram below shows IRQ 5 selected in a shared configuration. If no interrupt is desired, remove the jumper.

2	Selects IRQ2
3	Selects IRQ3
4	Selects IRQ4
5	Selects IRQ5
N	Selects Normal (1 IRQ per Board) IRQ Mode
M	Selects "Multi-IRQ" (Shared) IRQ Mode

The factory-default setting for E3 is "5" and "M."

EPROM Usage

The EPROM socket on the Serial Interface is provided for convenience only and does not affect the communication functions of the board in any way. If the EPROM is not used, the socket should be disabled (DIP switch SW2 position 5 off). The table below shows several EPROM base address examples.

The EPROM is a 27128 device occupying 16 KB of memory at or above C800 Hex to be recognized by the PC on bootup. Address lines A19 and A18 are always a binary 1, forcing a selection of C000 Hex or greater.

Address	Address Lines				Switch Position Setting (SW1)			
	A17	A16	A15	A14	1	2	3	4
C000-C3FF	0	0	0	0	ON	ON	ON	ON
C400-C7FF	0	0	0	1	ON	ON	ON	OFF
C800-C9FF	0	0	1	0	ON	ON	OFF	ON
D000-D3FF	0	1	0	0	ON	OFF	ON	ON
D400-D7FF	0	1	0	1	ON	OFF	ON	OFF
D800-DBFF	0	1	1	0	ON	OFF	OFF	ON
E000-E3FF	1	0	0	0	OFF	ON	ON	ON
E400-E7FF	1	0	0	1	OFF	ON	ON	OFF

NOTE

Some AT® class machines cannot use address E000 and above.

The table above illustrates the correlation between the DIP-switch setting and the address bits used to determine the base address.

Switch position 5 enables and disables the EPROM socket. The default setting is with the EPROM socket disabled.

The Serial Interface is shipped with all the positions of SW1 turned off. If you use the EPROM socket, make sure you change the setting of SW1 to the address range you need.
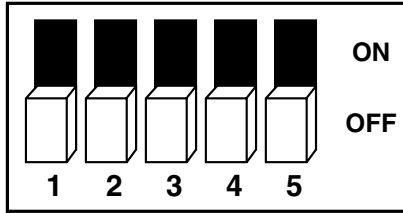
Figure 4-1. DIP Switch.

4.2 E1 and E2

E2 selects DMA mode of operation. Channel A of the SCC can be run in half-duplex or full-duplex DMA mode. Full-duplex DMA can transmit and receive data simultaneously. Half-duplex DMA can transmit, or receive data, but not in both directions simultaneously. Both Channels A and B can be used in half-duplex mode. The various options for E1 and E2 jumper settings are as follows:

NOTE

If DMA is not used, remove all of the jumpers on E1 and E2. Refer to page 13 for the most common DMA settings.
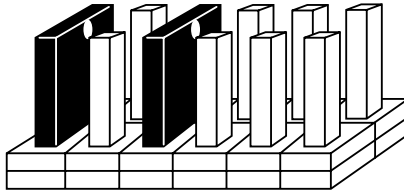

Figure 4-2. Header E2 DMA Mode Options.

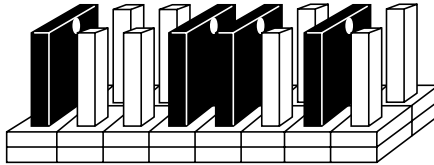| 1	DACK 1 or 3 Acknowledge for Two-Channel Mode
2	Two-Channel A/B Mode A3B1
3	Two-Channel A/B Mode A1B3
4	On = Ch. A Only/Off = Ch. B Only
5	DACK 3 DMA Acknowledge Channel 3
6	DACK 1 DMA Acknowledge Channel 1

Figure 4-3. Header E1 DMA Mode Options.

1	A or B Ch. 3
2	A only Ch. 3
3	A or B Ch.1
4	A only Ch. 1
5	B Enable
6	A Full Duplex
7	DMA Always Enabled
8	Control Port Bit 7 Enables DMA (see below)

E1 positions 7 and 8 enable or disable DMA operation. A jumper "ON"
position 7 permanently enables the DMA tri-state drivers. A jumper "ON"
position 8 places DMA under software control via the DMA enable control
port bit (located at Base+4). Removing the jumper disables the drivers and no
DMA can be performed.

NOTE

The power-on reset signal disables the DMA enable signal. A jumper placed in position 7 of E1 will override any software uses of the DMA enable/disable status-port bit.

Table 2. Commonly Used DMA Jumper Options

Option	Jumpers on E2	Jumpers on E1	Program 85230
No DMA Ch. A or B	None	None	N/A

Single-Channel DMA (Half-Duplex Only):

Option	Jumpers on E2	Jumpers on E1	Program 85230
Ch.A. DMA Ch. 1 Half-Duplex Ch. B No DMA	4, 6	4	WAIT/REQ A
Ch.A. DMA Ch. 3 Half-Duplex Ch. B No DMA	4, 5	2	WAIT/REQ A
Ch.B. DMA Ch. 1 Half-Duplex Ch. A No DMA	6 only	3, 5	WAIT/REQ B
Ch.B. DMA Ch. 3 Half-Duplex Ch. A No DMA	5 only	1, 5	WAIT/REQ B

Both DMA Channels (1 and 3) Selected:

Option	Jumpers on E2	Jumpers on E1	Program 85230
Ch. A DMA Ch. 1 Half-Duplex Ch. B DMA Ch. 3 Half-Duplex	1, 3	1, 4, 5	WAIT/REQ A WAIT/REQ B
Ch. A DMA Ch. 3 Half-Duplex Ch. B DMA Ch. 1 Half-Duplex	1, 2	2, 3, 5	WAIT/REQ A WAIT/REQ B

Full-Duplex DMA Channel A with Both DMA Channels 1 and 3:

Option	Jumpers on E2	Jumpers on E1	Program 85230
Ch. A DMA Ch. 1 Receive Data Ch. A DMA Ch. 3 Transmit Data	1, 4	1, 4, 6	WAIT/REQ A DTR/REQ A
Ch. A DMA Ch. 3 Receive Data Ch. A DMA Ch. 1 Transmit Data	1, 4	2, 3, 6	WAIT/REQ A DTR/REQ A

NOTE: Channel B of the Serial Interface does not support full-duplex DMA.

5. Installation

NOTE

Be sure to set the address selections and jumper options *before* installation.

The Dual Channel HS Sync/Async V.35 Serial Interface can be installed in any of the PC expansion slots.

1. Remove the PC case.

2. Remove the blank metal slot cover.

3. Gently insert the board.

4. Replace the screw.

5. Replace the cover.

Installation is complete.

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