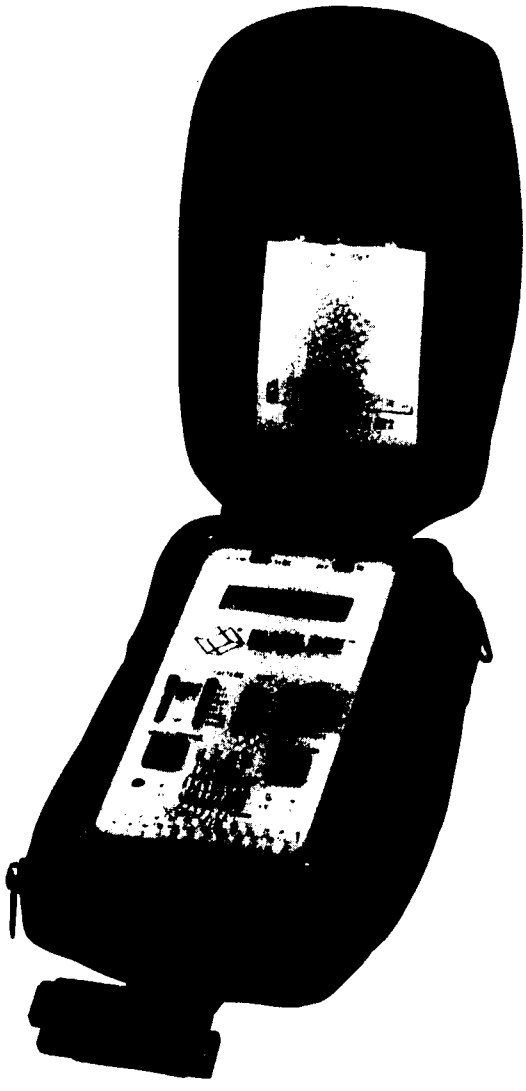
FAX COPY 22183

BLACK BOX Corporation
A MICOM COMPANY

DT003-1285

13 APR 1992

DATA CONTESTER
BERT/BLERT



CUSTOMER SUPPORT INFORMATION

Call our technical support specialist to discuss your application. We have a 30 day money-back guarantee.
For technical support call: (412) 746-5565 8:30 a.m. to 6:00 p.m. (Eastern)
To order call: (412) 746-5530 8:00 a.m. to 8:00 p.m. (Eastern)
Mail Order: **BLACK BOX Corporation**, Mayview Road at Park Drive, Box 12800, Pittsburgh, PA 15241

TABLE OF CONTENTS

FIGURES AND TABLES

INTRODUCTION

The ET-1 Error Rate Test Set is one of the finest engineered products in the world. As you become familiar with this instrument you will see the great care we have taken to provide you the features, ease-of-use, and flexibility that your work demands.

The ET-1 Error Rate Test Set is used to isolate faulty components and measure transmission quality in a communications network. It performs this function by comparing what it receives from the communication link to what it (or another ET-1) sent to the communication link. This comparison directly yields the accuracy and quality of the link being tested. This measure of quality is expressed in one of three industry accepted formats:

- Bit Error Rate
- Block Error Rate
- Errored Seconds Rate

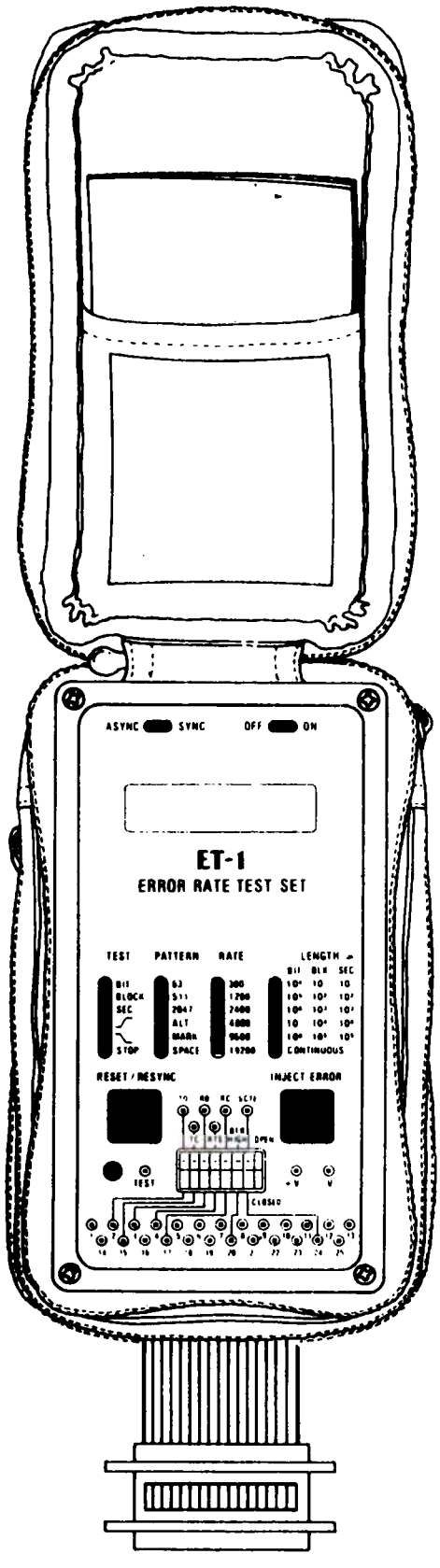
ET-1 gives you a choice of any of the above three tests along with a selection of test lengths so you can test to the accuracy you desire. In addition, ET-1 allows you to monitor any RS-232-C signal for either positive or negative transitions. This is handy for isolating intermittent control signal problems.

Great care has been taken to simplify every aspect of the operation of this instrument. The faceplate is clearly labeled so all functions are easy to locate and use. Test selections and their associated lengths have been color keyed for accuracy. Indication is given when a test is in progress and when it has been completed, so you have confidence in the progress of the test. A handy bi-color LED is located close to the connector pins to verify RS-232-C signals. A bank of DIP switches has been provided so you can easily modify the ET-1's standard "DTE" configuration to the configuration of your choice. Also, The RS-232-C connector is dual-gender (male and female), so you don't waste time fumbling for adapters.

FEATURES AND SPECIFICATIONS

- **Test Capablity:** Bit error rate testing, block error rate testing, errored second testing, positive transition counting, negative transition counting.
- **Test Length Selection:** Preset test lengths allow true error rate measurements. Display shows exact error rate at the completion of the test. No need for external rate calculations.
- **Test Lengths:** Bit error rate testing: 10^4, 10^5, 10^6 10^7, 10^8 bits, or continuous
  Block error rate testing: 10, 10^2, 10^3 10^4, 10^5 blocks, or continuous
  Errored seconds testing: 10, 10^2, 10^3 10^4, 10^5 seconds, or continuous
- **Test Data Patterns:** Pseudorandom bit patterns of lengths 63, 511, or 2047 bits, alternating mark/space, all mark, all space.
- **Baud Rate Selections:** 300, 1200, 2400, 4800, 9600, or 19,200 bps
- Synchronous or Asynchronous operation
- End-to-end or loopback testing
- Automatic compensation for transmission delay
- Single bit error injection for test verification
- **Error Rate Display:** 4 digit LCD with overflow and test state indications.
- **RS-232-C Breakout Functions:** Jumper post access to all 25 RS-232-C pins.
  Dip switches open any test set connection. When closed, tester is configured as DTE device.
  All test set input/output signals available at jumper posts to allow cross connection to any RS-232-C pin.
  High impedance, bi-color test LED to monitor any RS-232-C lead.

	Positive and negative voltages (EIA space and mark levels) provided to simulate control signals.
• Interface:	RS-232-C, V. 24, male and female connectors on attached ribbon cable. Normal configuration as DTE device.
• Power:	Two 9 volt alkaline batteries included will provide over 100 hours continuous use. (Duracell replacement batteries recommended).
• Physical Characteristics:	Durable vinyl SoftPak case, zipper access to front panel, cable, and battery compartments. Acrylic front panel with back-screened legends High impact inner plastic case.
• Dimensions:	7" L x 4.5" W x 2" D
• Weight:	17 oz.


ASYNC
SYNC
OFF
ON
ET-1
ERROR RATE TEST SET
TEST
PATTERN
RATE
LENGTH
BIT
BLOCK
SEC
STOP
63
511
2047
ALT
MARK
SPACE
300
1200
2400
4800
9600
19200
BIT
BLK
SEC
CONTINUOUS
RESET / RESYNC
INJECT ERROR
TEST
CLOSED

GENERAL DESCRIPTION

The ET-1 Error Rate Test Set is used to measure and troubleshoot digital data transmission errors on communication channels. It may be used to determine bit error rates, block error rates, errored second rates, or count transitions of either polarity on any RS-232-C interface pin.

The unit consists of a digital transmitter, receiver, and error counter. The transmitter circuit generates one of six selected serial bit patterns and drives the RS-232-C TD pin (typically pin 2). The receiver circuit generates an identical bit pattern and compares it with the incoming data stream on RD (typically pin 3). Whenever an incoming bit does not match the expected bit pattern, one bit error is counted.

The bit error rate is a measurement of the total number of bits in error related to the total number of bits transmitted, typically expressed in errors in 10^6 bits, 10^7 bits, etc.

Block error rate testing is used to emulate block message data transmission. For test measurements, a block is defined as 1000 bits and a block error is a group of 1000 bits that has one or more errors in it. Since errors typically come in bursts rather than by single bits, the block error rate gives a better indication of the percentage of message blocks that would have to be retransmitted due to errors than calculations based on the bit error rate. The block error rate is similarly expressed in errors in 10^3 blocks, 10^4 blocks, etc.

Errored second (or error-free second) testing indicates valid data transmission per unit time, rather than by number of bits or blocks transmitted, and is thus independent of the transmission rate. An errored second is a second of transmission time in which one or more errors have been received. Conversely, error-free seconds are units of time that have no transmission errors. The ET-1 records errored seconds, since this number is much smaller than error-free seconds and is less likely to overflow the error counter. To convert to error-free seconds, the number of errored seconds is simply subtracted from the total test length.

The test pattern selections for error rate testing include industry standard pseudorandom bit patterns of length 63, 511, or 2047 bits, alternating mark/space, all mark, or all space patterns. The pseudorandom patterns have statistical properties

which approximate real world random data streams. These patterns repeat after the specified length; therefore, the longer the sequence, the better it approximates random data. As faster data rates are used, longer pseudorandom sequences should be selected to optimize random data simulation. Since these pseudorandom patterns are standard with other bit error rate testers, the ET-1 may be used in end-to-end testing with equipment from other manufacturers as well as another ET-1.

Test lengths may be selected so that after a preselected number of bits or blocks have been received or after a preselected number of test seconds have passed, the error count is stopped. The count displayed at the end of the test is the number of errors counted over the selected test length, directly readable as the error rate. For example, if a bit error test of length 10^5 bits is selected and the display reads "5" at the end of the test, the bit error rate is 5 in 10^5 bits or .00005.

The test length counter, as well as the error counter is reset at the start of the test by pushing the RESET/RESYNC button. During the test, the arrow indicator in the upper left corner of the error display flashes to indicate test in progress. At the completion of the test, the arrow stays on steady and the counter displays the error rate. If there are no errors, the display goes blank.

When the RESET/RESYNC button is pushed, the receiver section synchronizes with the incoming data stream. Since the transmitter and receiver circuits are functionally independent within the unit, transmission delays between the transmitted data and the received data are automatically compensated.

In the transition counting mode, the ET-1 counts positive or negative transitions detected on the RD pin. When the DIP switches in the breakout section are opened, the RD input may be jumpered to any RS-232-C interface pin to monitor control signal transitions. The dual-gender RS-232-C connector allows the ET-1 to be easily inserted between communicating devices and monitor control transitions without interfering with data transmission. A typical use of this function might be to monitor loss of Data Carrier Defect in a modem connection over an extended period of time.

OPERATING CONTROLS AND DISPLAYS
(Refer to Figure 1)

1. **ON/OFF**—Unit power switch.
2. **ASYNC/SYNC**—Selects asynchronous or synchonous mode of transmission.
3. **Error Display**—Indicates number of bit errors, block errors, errored seconds, or transtitions, depending on test selected. "+" indicates counter overflow (loss of sync.). Arrow flashes while test is in progress, lights steady when ready for test or when test is complete. Leading zeros are blanked when test is complete. Blank count display indicates no errors.
4. **TEST**—Selects type of test to perform:
   - BIT = Bit error rate test
   - BLOCK = Block error rate test
   - SEC = Errored second test
   - ⌐‾ = Positive edge transition counting
   - ‾⌐ = Negative edge transition counting
   - STOP = Stop transmission; TD=Mark, RTS=OFF, Clear Display
5. **PATTERN**—Selects data pattern that is transmitted:
   - 63 = 63 Bit long pseudorandom bit pattern
   - 511 = 511 Bit long pseudorandom bit pattern
   - 2047 = 2047 Bit long pseudorandom bit pattern
   - ALT = Alternating 1/0 pattern
   - MARK = All Mark (Logic "1") transmission
   - SPACE = All Space (Logic "0") transmission
6. **RATE**—Selects baud rate: 300 – 19,200 BPS
7. **LENGTH**—Selects length of test to perform. Color coded columns indicate the test length selection (in number of bits, blocks, or seconds) for the type of test that is selected. The error count is stopped and displayed when the selected test length has been counted by the receiver. Continuous selection allows continuous counting (test does not stop).
8. **RESET/RESYNC**—Resets error count, initializes test length count and synchronizes receiver with incoming data stream. Used to begin a test.

9. **INJECT ERROR**—Injects a single bit error in the transmitted data stream. Used to verify test set-up.

10. **Tester I/O Pins**—Inputs and outputs from tester. Normally connected through dip switches to RS-232-C pins as shown on faceplate.

11. **Dip Switches**—Open individual signal leads between tester and RS-232-C connector. When switches are in the CLOSED position, ET-1 is configured as a standard DTE device. The right-most switch position is not used.

12. **TEST LED**—Indicates voltage at test pin. May be jumpered to any RS-232-C lead. LED lights green for Mark (Control off, negative voltage) condition, red for Space (control on, positive voltage) condition, and both red and green for clocking condition.

13. **+V, –V Pins**—Provide EIA Mark and Space voltage levels. May be jumpered to RS-232-C control leads as needed for interface.

14. **RS-232-C Pins**—Jumper access pins to all 25 RS-232-C connector leads.

15. **Dual-gender RS-232-C connector**

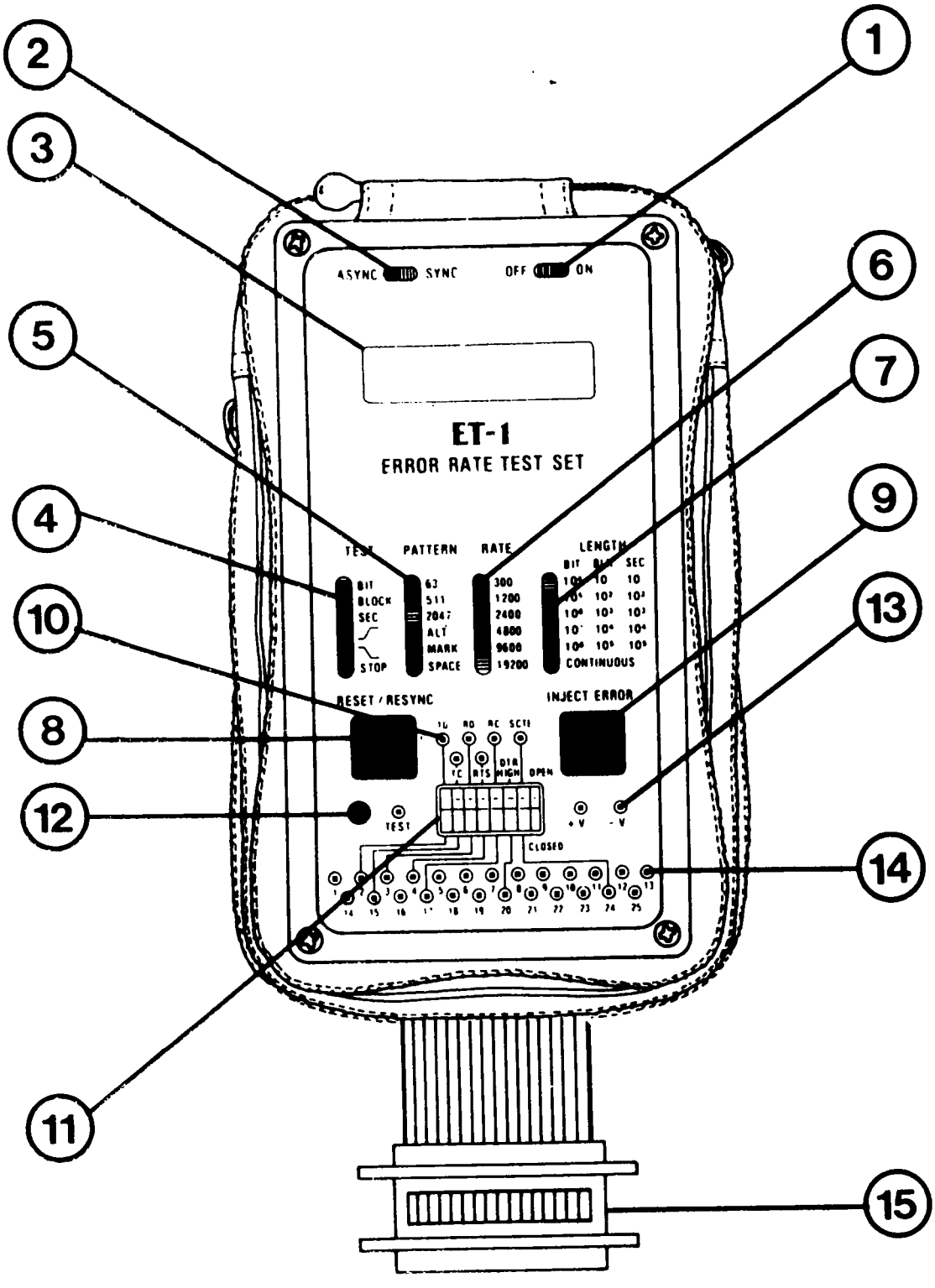


Figure 1. ET-1 Front Panel

ERROR RATE TEST CONFIGURATIONS

Figure 2 shows a typical terminal—modem—computer link. To test the transmission error rate of the link and isolate the faulty component, the ET-1 is substituted for the local terminal (DTE) device. Beginning with digital loop-back at the local modem, each portion of the transmission channel is successively looped-back and tested. The four standard loop-back configurations are shown in figure 3a-d. A faulty transmission channel may be identified when the error rate significally increases at that stage of loop-back.

With loop-back testing, however, it is not possible to identify whether the transmit channel or the receive channel is causing the transmission errors since the data stream is looped through both channels. If it is necessary to perform this level of fault isolation, then end-to-end testing with a second ET-1 at the remote interface must be used (Figure 4). Now errors registered at each test set indicate errors on the receive channel to that end of the transmission channel. Separate error rates may be measured for both the transmit and receive channels with this arrangement.

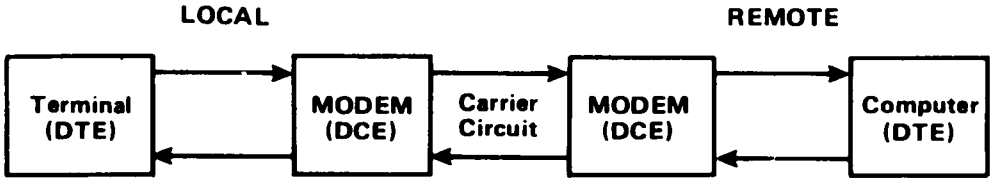


Figure 2. Typical Terminal—Modem—Computer Link

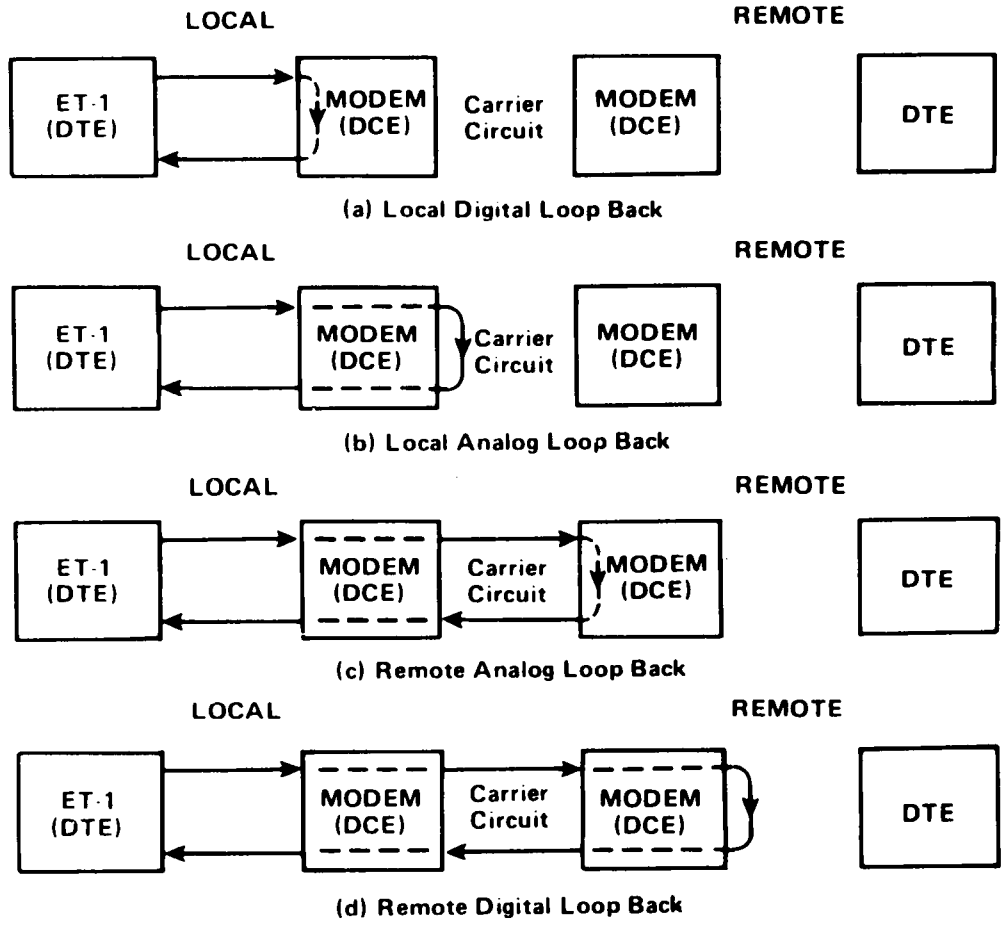


Figure 3. Loop-Back Testing

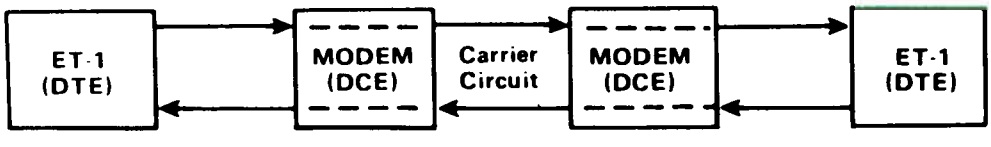


Figure 4. End-To-End Testing

SYNCHRONOUS ERROR RATE TESTING

1. Set ET-1 power switch OFF.
2. Set ASYNC/SYNC switch to SYNC.
3. Set TEST switch to either BIT, BLOCK, or SEC for appropriate test.
4. Set PATTERN switch for appropriate test (usually 63, 511, or 2047 pseudorandom patterns).
5. Set LENGTH switch for selected test length. Refer to Table 1 for test durations.
6. Close all interface DIP switches.
7. Disconnect terminal device from modem. Connect ET-1 to modem cable.
8. The modem should provide the transmitter clock on pin 15 and the receiver clock on pin17. The data bit rate is controlled by the modem. If the modem does not supply clock signals, the ET-1 provides an auxillary clock source on pin 24 (SCTE) which may be used internally by the modem or jumpered on the ET-1 to pins 15 and 17. The SCTE clock rate is selectable between 300 and 19,200 baud by the RATE switch.
9. If in doubt, modem signals may be verified by jumpering to the TEST PIN (after the power switch is turned ON). The TEST LED will light GREEN for a MARK (control OFF) condition, RED for a SPACE (control ON) condition, and both RED and GREEN for a CLOCKING condition. Do not leave the TEST LED connected for the duration of the test as this will shorten the battery life.
10. To connect to non-standard modem pin-out configurations, open the DIP switches and jumper ET-1 I/O pins to appropriate RS-232-C pins. Additional modem control pins may be jumpered to +V or –V voltage terminals (EIA space and mark levels) as needed.
11. Set ET-1 power switch ON. Arrow will light steady in upper left corner of error display. ET-1 will transmit data until unit is turned off or test switch is set to STOP position.

12. Set transmission channel for loop-back testing or establish connection with remote test set (end-to-end testing). Incoming data stream may be verified on RD pin by jumpering to the TEST pin.

13. Push RESET/RESYNC button to begin test. The error display will show "0000" with a flashing arrow. The error count will increment as each error is detected. If the counter is incrementing rapidly (with each received data unit), the receiver is not synchronized with the transmitted data. Verify data connections to modem and loop-back configuration, and push RESET/RESYNC button again to resynchronize receiver.

14. Single bit errors may be injected into the transmitted data stream to verify transmission connection. In loop-back testing, the error count should increment each time the INJECT ERROR button is pushed. With end-to-end testing, errors injected at one end will be counted on the opposite end.

15. When the test is complete, the arrow will light steady and the error rate will be displayed with leading 0's blanked. If no errors were detected, the error count will be blank. A "+" to the left of the error count indicates counter overflow (usually due to loss of sync.).

ASYNCHRONOUS ERROR RATE TESTING

1. Set ET-1 power switch OFF.
2. Set ASYNC/SYNC switch to ASYNC.
3. Set TEST switch to either BIT, BLOCK, or SEC for appropriate test.
4. Set PATTERN switch for appropriate test. For the 63, 511, and 2047 pseudorandom patterns, no start or stop bits are injected in the data stream (this would invalidate the "randomness" of the sequence). If the transmission system being tested requires start/stop bits, the ALT pattern must be used. The ALT pattern is interpreted as an ASCII "U" character with 7 bit data, even or space parity, and one stop bit (or 8 bit data, no parity and one stop bit).
5. Set LENGTH switch for selected test length. Refer to Table 1 for test durations.
6. Close all interface DIP switches.
7. Set RATE switch for appropriate baud rate.
8. Disconnect terminal device from modem. Connect ET-1 to modem cable. The ET-1 is configured as a DTE device; it transmits data on pin 2 and receives data on pin 3 of the RS-232-C interface.
9. If in doubt, modem signals may be verified by jumpering to the test pin (after the power switch is turned ON). The TEST LED will light GREEN for a MARK (control OFF) condition. RED for a SPACE (control ON) condition, and both RED and GREEN for a CLOCKING condition. Do not leave the TEST LED connected for the duration of the test as this will shorten the battery life.
10. To connect to non-standard modem pin-out configurations, open the DIP switches and jumper ET-1 I/O pins to appropriate RS-232-C pins. Additional modem control pins may be jumpered to +V or –V voltage terminals (EIA space and mark levels) as needed.
11. Set ET-1 power switch ON. Arrow will light steady in upper left corner of error display. ET-1 will transmit data

until unit is turned off or test switch is set to STOP position.

12. Set transmission channel for loop-back testing or establish connection with remote test set (end-to-end testing). Incoming data stream may be verified on RD pin by jumpering to the TEST pin.

13. Push RESET/RESYNC button to begin test. The error display will show "0000" with a flashing arrow. The error count will increment as each error is detected. If the counter is incrementing rapidly (with each received data unit) the receiver is not synchronized with the transmitted data; verify data connections to modem and loop-back configuration and push RESET/RESYNC button again to resynchronize receiver.

14. Single bit errors may be injected into the transmitted data stream to verify transmission connection. In loop-back testing, the error count should increment each time the INJECT ERROR button is pushed. With end-to-end testing, errors injected at one end will be counted on the opposite end.

15. When the test is complete, the arrow will light steady and the error rate will be displayed with leading 0's blanked. If no errors were detected, the error count will be blank. A "+" to the left of the error count indicates counter overflow (usually due to loss sync.).

TRANSITION MONITORING

1. Set ET-1 power switch OFF.
2. Set TEST switch to ⎍ to count positive voltage transitions (mark-to-space), or ⎺⎺__ to count negative voltage transitions (space-to-mark).
3. Open all interface DIP switches.
4. Connect ET-1 in series between DTE and DCE devices with the dual-gender RS-232-C connector. The DTE will be connected to the DCE through the ET-1.
5. Jumper RD (counter input) to the RS-232-C lead to be monitored.
6. Set LENGTH switch to CONTINUOUS. If testing over a preset period of time is desired, set LENGTH switch to obtain desired test duration (read SEC column).
7. Set ET-1 power switch ON. Push RESET/RESYNC button to begin test. The display will initially show "0000" and will increment with each transition. The arrow in the upper left corner of the display will flash while the test is running.

SELF TEST

1. Disconnect ET-1 RS-232-C cable from external equipment.
2. Set ASYNC/SYNC switch to ASYNC.
3. Set TEST switch to BIT to count bit errors.
4. Set PATTERN switch to 63.
5. Set RATE switch to 19200.
6. Set LENGTH switch to CONTINUOUS.
7. Jumper TD pin to RD pin. This loops back the transmitted data stream to the receiver.
8. Set power switch ON. Arrow should light steady.
9. Push RESET/RESYNC button to start bit error test. Display should read "0000" with a flashing arrow. Transmitter and receiver circuits are now synchronized.
10. Push INJECT ERROR button to insert errors in data stream. Count should increment each time button is pushed.
11. Jumper SCTE pin to TC and RC pins with 4-way bridging jumper to provide synchronous transmitter and receiver clocks. TD and RD are still jumpered.
12. Set ASYNC/SYNC switch to SYNC.
13. Push RESET/RESYNC button to resynchronize receiver. Display should read "0000" with a flashing arrow.
14. Push INJECT ERROR button to insert errors in data stream. Count should increment each time button is pushed.
15. Remove jumper from RD pin. Counter should increment rapidly. Reconnect RD jumper. Error count should stop incrementing.
16. Set Length switch to 10^4 bits.
17. Push RESET/RESYNC button to start bit error test. Display should flash "0000" for one second then go blank, indicating no errors.

18. Remove jumper between TD and RD. Jumper RD to –V (solid mark level).

19. Push RESET/RESYNC button to start each bit error test. Tester error count at end of test should read:

    4923 for the 63 pattern
    4997 for the 511 pattern
    5001 for the 2047 pattern
    5000 for the ALT pattern
    Blank (0 errors) for the MARK pattern
    +0000 (overflow) for the SPACE pattern

    These counts verify test data patterns.

20. Set TEST switch to BLOCK to count block errors.

21. Set PATTERN switch to 63. LENGTH switch is set to 10 blocks.

22. Push RESET/RESYNC button to start block error test. Tester should count 10 block errors.

23. Set LENGTH switch to 10^2 blocks. Push RESET/RESYNC button to start block error test. Tester will count block errors.

24. Move RATE switch to slower baud rates. Count should increment at a slower rate. Counter should stop at 100 block errors.

25. Set TEST switch to SEC to count errored seconds. Set LENGTH switch to 10 seconds.

26. Push RESET/RESYNC switch to start errored second test. Tester should increment every second to a final count of 10 errored seconds.

27. Set TEST switch to ⎍. Set PATTERN switch to SPACE. Set LENGTH switch to CONTINUOUS. Remove jumper from SCTE, TC and RC pins. RD is jumpered to –V. Push RESET/RESYNC button to start transition count test. Display should read "0000" with flashing arrow.

28. Remove RD jumper from –V terminal and touch to +V terminal. Count should increase each time +V terminal

is touched. **NOTE:** The high-impedance RD input may respond to noise when disconnected (open), creating false transition counts.

29. Set TEST switch to ⎍ . Touch RD jumper to +V terminal. Count should increase each time +V terminal is touched.

30. Jumper RTS pin to TEST pin. TEST LED should light RED, indicating control ON condition for RTS.

31. Set TEST switch to STOP. Test LED should light GREEN, indicating control OFF condition for RTS. Display count should go blank, arrow should light steady.

32. Remove jumper and turn power switch OFF. Test complete.

Table 1. TEST DURATIONS

LENGTH		BAUD RATE					
BIT	BLK	300	1200	2400	4800	9600	19,200
10^4	10	33 sec	8 sec	4 sec	2 sec	1 sec	.5 sec
10^5	10^2	5.5 min	83 sec	42 sec	21 sec	10 sec	5 sec
10^6	10^3	56 min	14 min	7 min	3.5 min	2 min	52 sec
10^7	10^4	9 hr, 16 min	2 hr, 19 min	1 hr, 9 min	35 min	17 min	9 min
10^8	10^5	92 hr, 36 min	23 hr, 9 min	11 hr, 35 min	3 hr, 47 min	2 hr, 54 min	1 hr, 27 min

LENGTH SEC	DURATION
10	10 sec
10^2	1 min, 40 sec
10^3	16 min, 40 sec
10^4	2 hr, 47 min
10^5	27 hr, 47 min

TABLE 2
EIA/CCITT MODEM–TERMINAL INTERFACE

PIN	NAME	FUNCTION	SOURCE	CIRCUIT EIA/CCITT
1	FG	FRAME GROUND	——	AA/101
2	TD	TRANSMITTED DATA	DTE	BA/103
3	RD	RECEIVED DATA	DCE	BB/104
4	RTS	REQUEST TO SEND	DTE	CA/105
5	CTS	CLEAR TO SEND	DCE	CB/106
6	DSR	DATA SET READY	DCE	CC/107
7	SG	SIGNAL GROUND	——	AB/102
8	DCD	DATA CARRIER DETECT	DCE	CF/109
9		POSITIVE TEST VOLTAGE	DCE	
10		NEGATIVE TEST VOLTAGE	DCE	
11	QM	EQUALIZER MODE	DCE	BELL 208A
12	SDCD	SEC. DATA CARRIER DETECT	DCE	SCF/122
13	SCTS	SEC. CLEAR TO SEND	DCE	SCB/121
14	STD	SEC. TRANSMITTED DATA	DTE	SBA/118
	NS	NEW SYNC.	DTE	BELL 208A
15	TC	TRANSMITTER CLOCK	DCE	DB/114
16	SRD	SEC. RECEIVED DATA	DCE	SBB/119
	DCT	DIVIDED CLOCK, TRANSMIT	DCE	BELL 208A
17	RC	RECEIVER CLOCK	DCE	DD/115
18	DCR	DIVIDED CLOCK, RECEIVE	DCE	BELL 208A
19	SRTS	SEC. REQUEST TO SEND	DTE	SCA/120
20	DTR	DATA TERMINAL READY	DTE	CD/108.2
21	SQ	SIGNAL QUALITY DETECT	DCE	CG/110
22	RI	RING INDICATOR	DCE	CE/125
23	DRS	DATA RATE SELECTOR	DTE	CH/111
		DATA RATE SELECTOR	DCE	CI/112
24	SCTE	SERIAL CLK TRANSMIT EXT.	DTE	DA/113
25	BUSY	BUSY	DTE	BELL 1138

RED = POSITIVE VOLTAGE, BINARY ZERO, SIGNAL SPACE, CONTROL ON
GREEN = NEGATIVE VOLTAGE, BINARY ONE, SIGNAL MARK, CONTROL OFF